IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of: Klaus Florian Schuegraf, Scott J. DeBoer and Randhir P. S. Thakur

Title: SELECTIVE SPACER TECHNOLOGY TO PREVENT METAL OXIDE FORMATION DURING POLYCIDE REOXIDATION

Docket No.: 303.278US1

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United States Patent Application

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As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **SELECTIVE SPACER TECHNOLOGY TO PREVENT METAL OXIDE FORMATION DURING POLYCIDE REOXIDATION**.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

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I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Randhir P.S. Thakur

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(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

SELECTIVE SPACER TECHNOLOGY TO PREVENT METAL OXIDE FORMATION DURING POLYCIDE REOXIDATION

Field of the Invention

The present invention relates in general to fabricating semiconductor devices, and particularly to controlling oxide formation during reoxidation.

Background of the Invention

Advancing technology continues to pressure manufacturers to produce complementary metal-oxide semiconductor (CMOS) devices with both greater capacities and smaller profiles. To counteract the resulting parasitic effects caused by resistance/capacitance delays in gate electrodes in such down-scaled devices, there is a continual quest for new combinations of materials from which to fabricate gate structures. For example, in *W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs*, 497-500 **IEDM 1994**, K. Kasai et al. describe a structure comprising tungsten, tungsten nitride and polysilicon (W/WNx/PolySi). This structure has a greatly reduced sheet resistance and enables improved performance of the CMOS device. The structure proposed by Kasai et al. is, however, limited because the structure is only able to withstand temperatures up to 900°C for 30 seconds or less during rapid thermal annealing. Proper source/drain reoxidation requires temperatures at or above 900°C for at least fifteen minutes. To date, where the W/WNx/PolySi structure is used, after source/drain reoxidation the wordline profile exhibits a considerable protuberance on the exposed tungsten silicide (WSi_x). This complicates subsequent etches, and the undesirable "spacer" implants from the gate edge decrease device performance.

In conventional processing, a conductive gate electrode is patterned into fine features by photo/etch processing. This electrode is subsequently subjected to reoxidation to repair physical damage caused by the etch process in one of two ways: either directly or through a deposited silicon dioxide spacer. For a tungsten silicide feature, this reoxidation results in SiO_2 growth on the polysilicon and silicide. Other

choices for metal shunt layers of polysilicon include materials such as tungsten, titanium silicide and molybdenum. As described by Robert Beyers in *Thermodynamic considerations in refractory metal silicon-oxygen systems*, 147-52 **Journal of Applied Physics 56(1)**, (July, 1984), these metals, when oxidized, result in unstable metal oxides. This is because, unlike tungsten silicide, there is little or no silicon available for oxidation into SiO_2.

As a result, there remains a need to be able to tap the potential of devices manufactured from materials such as tungsten and minimize the detrimental effects resulting from the formation of oxide.

Summary of the Invention

The primary object of the present invention is to eliminate the aforementioned drawbacks of the prior art.

This invention proposes a method for forming an encapsulating spacer for protecting a refractory metal or polycide from forming metal oxide formation during gate stack reoxidation. According to one embodiment an encapsulating spacer is formed prior to gate stack reoxidation to prevent undesirable formation of metal oxides during this oxidation process. In another embodiment either a thin silicon nitride or amorphous silicon film is selectively deposited after gate stack patterning over a gate stack without any deposition on the active areas. This selective deposition will result in a thin film of insulating material over the gate stack which will prevent metal oxide formation during polycide (source/drain) reoxidation.

The present invention describes an improvement in the one-spacer approach because it allows source/drain reoxidation after patterning. Conventional processes using tungsten or tungsten nitride experience a "rabbit ear" problem of tungsten reoxidation after any thermal cycle more intensive than rapid thermal annealing performed at temperatures higher than 900°C.

The present invention also describes an improvement in the two-spacer approach, simplifying the double spacer deposition/etch sequence into a sequence

comprising two depositions and one etch. Yet another embodiment of the present invention encapsulates refractory metal from uncontrollable oxidation during source/drain reoxidation after gate patterning.

Brief Description of the Drawings

Figure 1 is a graphic representation of the physical phenomena to be exploited for the selective spacer process.

Figure 2A is a cross-sectional view of a portion of an in-process semiconductor wafer following gate line masking and a subsequent dry etch of the exposed silicon nitride, using the polysilicon layer as the etch stop.

Figure 2B is a cross-sectional view of the portion of an in-process semiconductor wafer depicted in Figure 2A following selective spacer deposition according to one embodiment of the present invention.

Figure 2C is a cross-sectional view of the portion of an in-process semiconductor wafer depicted in Figure 2B following reoxidation.

Figure 2D is a cross-sectional view of a portion of an in-process semiconductor wafer after selective spacer deposition and reoxidation, wherein the gate line is formed of undoped silicon.

Detailed Description of the Preferred Embodiments

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

In conventional processing, reoxidizing a device results in silicon dioxide growth on both polysilicon and silicide features. As mentioned above, this creates an unacceptably deformed wordline profile. According to one embodiment of the present invention, the deformation is minimized by selective spacer formation on the sidewalls of tungsten silicide features. The spacer minimizes oxidation and the subsequent degradation of the feature.

Figure 1 provides a graphic representation of the physical phenomena which the selective spacer process employs. The example presented shows that deposition of spacer materials on polysilicon 110 occurs more rapidly than deposition on oxide 120. Those skilled in the art will recognize that other materials may be used in place of polysilicon with similar results. The difference in incubation time 130 on dissimilar materials makes selective spacer deposition possible. For both silicon nitride and undoped polysilicon, deposition parameters (temperature, pressure, flow rates, etc.) can be adjusted to provide a rather wide incubation time difference 130. For example, in one embodiment where Si_3N_4 is deposited as the spacer material, a deposition difference as high as 60 Angstroms can be achieved for film deposition on different surfaces (such as silicon dioxide and silicon or polysilicon) using a temperature of 680°C, a pressure of 80 milliTorrs, and a flow ratio of 6:1.

Figures 2A-2D show how this incubation time difference 130 can be exploited for selective spacer deposition, encapsulating refractory metal prior to polycide reoxidation. As shown in Figure 2A, the first step is patterning an electrode 205 into fine feature. In the embodiment shown in figure 2A electrode 205 comprises nitride. Those skilled in the art will recognize, however, that other materials, such as undoped silicon, may be used to construct electrode 205. In the second step, represented in Figures 2B and 2C, a selective spacer 210 is deposited such that the amount deposited on the polysilicon and refractory metal 205 is less than the incubation thickness, leaving the active area 215 free of deposition. In one embodiment the spacer comprises a thin silicon nitride, while in another it comprises an amorphous silicon film. It is to be noted

that the foregoing examples are meant to be illustrative only and not limiting in any fashion.

Once the spacer is deposited, the device undergoes polycide reoxidation. Because the spacer is selectively deposited there is no need for an additional etch step to remove excess spacer material. The oxidation process forms smile 225, and active area 215 and selective spacers 210 are reoxidized. As can be seen, the metal portion of electrode 205 is protected by spacers 210 and thus is not subjected to the high temperature oxygen environment. Selective spacer 210 acts as a diffusion barrier preventing oxygen from reaching metal layers 205 of electrode 205. Subsequently, an additional spacer may be deposited to the desired spacer thickness of several hundred angstroms, setting the lateral dimension of the transistor's source/drain diffusion. As shown in Figure 2D, similar results are obtainable when electrode 205 comprises undoped silicon.

The net result is that the additional step of protecting the feature can be performed though modifying process parameters and without adding any further steps to the overall process. The process described enables devices fabricated from materials such as tungsten to be more fully exploited, minimizing detrimental effects resulting from the formation of oxide, and all without increasing the cost or complexity of the fabrication process. For example, if one spacer is desired source/drain reoxidation may be performed after patterning. In contrast, conventional processes (such as the W/WN_x stack described in the paper by Kasai et al.), will show a "rabbit ear" problem of tungsten reoxidation after a thermal cycle.

In a two-spacer approach, the method of the present invention simplifies the double spacer deposition/etch sequence into two deposition and one etch sequence. According to one embodiment, during source/drain reoxidation the refractory metal exposed by patterning is encapsulated, protecting the metal from uncontrollable oxidation. In contrast, conventional processing requires a deposition and etch step for each spacer before source/drain oxidation can be performed.

Is it to be recognized that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A method of fabricating a semiconductor device, having one or more layers of materials deposited on a polysilicon layer, comprising the steps of:

forming one or more features on the semiconductor device, each of the one or more features having sidewalls;

selectively depositing a first spacer on the sidewalls of each of the one or more features; and

reoxidizing the semiconductor device.

2. The method of claim 1, wherein the step of forming one or more features comprises selectively etching the one or more features having sidewalls, thereby exposing the one or more layers of materials.

3. The method of claim 2, wherein the polysilicon layer serves as an etch stop.

4. The method of claim 1, wherein the step of selectively depositing a first spacer further comprises limiting deposition time to be less than incubation time.

5. The method of claim 1, wherein the step of selectively depositing a first spacer comprises selectively depositing a thin silicon nitride.

6. A method of fabricating a semiconductor device, having one or more layers of materials deposited on a polysilicon layer, comprising the steps of:

selectively etching the semiconductor device to form one or more features having sidewalls exposing the one or more layers of materials, wherein the polysilicon layer serves as an etch stop;

selectively depositing a first spacer on the sidewalls of each of the one or more features; and

reoxidizing the semiconductor device.

7. The method of claim 6, wherein the step of selectively depositing a first spacer further comprises limiting deposition time to be less than incubation time.

8. The method of claim 6, wherein the step of selectively depositing a first spacer comprises selectively depositing a thin silicon nitride.

9. A method of forming a structure for controlling current flow between a source and a drain region in a semiconductor device, comprising the steps of:

forming an insulating layer on a semiconductor wafer;

forming a conductive layer over the insulating layer;

forming a gate by etching, using the insulating layer as an etch stop, wherein the gate has sidewalls exposing the conductive layer and some portion of the insulating layer;

selectively forming a first oxidation barrier on the sidewalls of the gate; and

reoxidizing the structure.

10. The method of claim 9, wherein the step of selectively forming a first oxidation barrier comprises selectively depositing a thin silicon nitride on the gate without depositing any on the source and the drain regions.

11. A method of forming a structure for controlling current flow between a source and a drain region in a semiconductor device, wherein the semiconductor device is composed of a semiconductor wafer, an insulating layer disposed over the semiconductor layer, and a conductive layer disposed over the insulating layer, the method comprising the steps of:

forming a gate having sidewalls exposing the conductive layer and some portion of the insulating layer;

depositing a thin silicon nitride on the gate;

avoiding depositing the thin silicon nitride on the source and the drain region;

forming a first oxidation barrier on the sidewalls of the gate; and

reoxidizing the structure.

12. The method of claim 11, wherein the step of avoiding depositing the thin silicon nitride on the source and the drain regions comprises limiting deposition time to be less than incubation time.

13. A semiconductor device, comprising:

a layer of polysilicon;

one or more active areas;

one or more features protruding from the polysilicon and having sidewalls, the one or more features separating the one or more active areas, each of the one or more features including:

a portion of the polysilicon layer,

one or more layers of conductive materials deposited on the layer of polysilicon, and

a spacer selectively deposited on the sidewalls of the one or more features; and

a layer of silicon oxide deposited on the semiconductor device, wherein the spacer is interposed between the layer of silicon dioxide and the sidewalls.

14. The semiconductor device of claim 13, wherein the selective spacer comprises silicon nitride.

15. The semiconductor device of claim 13, wherein the one or more layers of conductive materials comprise tungsten silicide.

16. A semiconductor device, comprising:

a layer of polysilicon;

one or more active areas; and

one or more features protruding from the polysilicon and having sidewalls, the one or more features separating the one or more active areas, each of the one or more features comprising:

one or more layers of conductive materials deposited on the layer of polysilicon, at least one layer of which includes tungsten silicide; and

a silicon nitride spacer selectively deposited on the sidewalls of the one or more features; and

a layer of silicon oxide deposited on the semiconductor device, wherein the silicon nitride spacer is interposed between the layer of silicon oxide and the sidewalls of the one or more features.

17. A gate electrode, comprising:

one or more layers of conductive materials etched to form features having sidewalls exposing the one or more layers;

a selectively deposited spacer, wherein the spacer is deposited only on the feature sidewalls;

a layer of silicon oxide disposed over the gate electrode surface.

18. The gate electrode of claim 17, wherein the one or more layers of conductive materials comprise tungsten silicide.

19. The gate electrode of claim 17, wherein the selectively deposited spacer comprises silicon nitride.

20. A semiconductor device having a device having an electrode and an active area, wherein the electrode has a side and the active area has a surface, comprising:

a spacer, wherein

the spacer covers the electrode; and

the spacer provides unobstructed physical communication with the active area.

21. The semiconductor device of claim 20, wherein:

the spacer covers the side of the electrode; and

the spacer provides unobstructed physical communication with the surface of the active area.

22. A spacer for a semiconductor device, wherein:

the spacer is disposed to substantially prevent physical communication between a first layer of the semiconductor device and a first area of the semiconductor device; and

the spacer is disposed to provide unobstructed physical communication between the first layer of the semiconductor device and a second area of the semiconductor device.

Abstract of the Disclosure

A method of forming an encapsulating spacer prior to gate stack reoxidation is provided which prevents the formation of undesirable metal oxides during reoxidation. A material such as a thin silicon nitride or amorphous silicon is selectively deposited by limiting deposition time to a period less than incubation time. As a result spacers are formed without having to perform an additional etch act.

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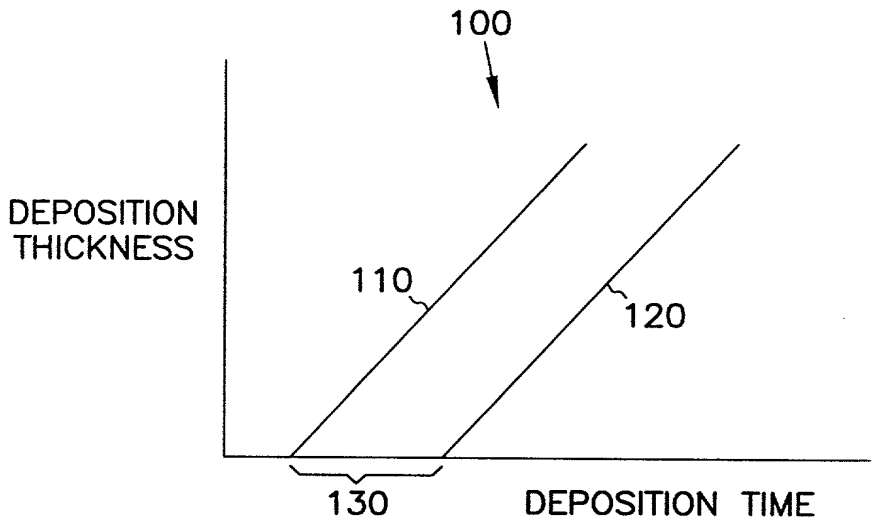

FIG. 1

FIG. 2A

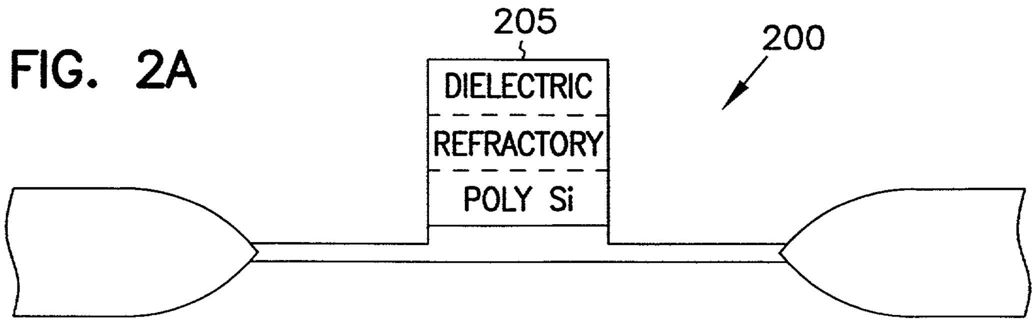

FIG. 2B

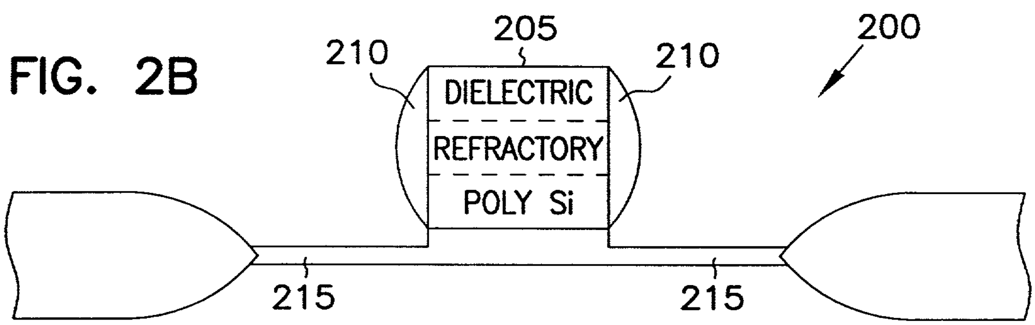

FIG. 2C

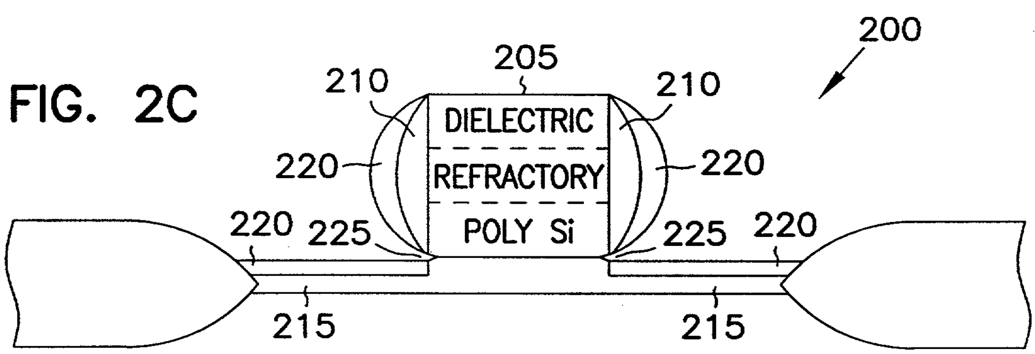

FIG. 2D